QET Bias Noise Specification

Revision 2MAR01 D. Seitz:

Changed Rbias from 4.99k to 2.49k to double bias range to +/-2mA.

The following values should be changed in the documents below:

Figure 1, Test Circuit 1:
Rbias = 2.49kΩ
VN8 = 6.4nV/√Hz

Test Circuit 1:
typical noise @SR770: 8µV/√Hz
max noise @SR770: 11µV/√Hz

Discussion:

The voltage noise of Rbias = 6.4nV/√Hz. Added to the 2.7nV/√Hz from the bias circuit gives a total Vnoise of 6.9nV/√Hz @ 125Hz.
6.9nV/√Hz/2.49kΩ = 2.8pA/√Hz at 125Hz expected current noise instead of the original 1.9pA/√Hz.

A 40mΩ shunt resistance and 100mΩ QET resistance gives an expected input coil Inoise of 0.8pA/√Hz instead of the original 0.7pa/√Hz max spec, so we will exceed the max spec by at least 14%.
However, if the shunt resistance is assumed to be <<40mΩ the original spec is still met. With a 30mΩ shunt, for instance, the expected QET noise current is 0.65pA/√Hz, within the original spec. Measurements at UCB have indicated that the shunt resistance is very close to the nominal 20mΩ. Additionally, QET noise is on the order of 10pA/√Hz so even if the shunt resistor were >20mΩ the QET bias noise would not significantly alter noise performance.

The test setup max voltage noise spec is actually reduced with the 2.49k Rbias value. The typical noise expected at the SR770 is now 8µV/√Hz.
Assuming a nominal 20mΩ shunt the max allowable noise at the SR770 is now 11µV/√Hz @ 125Hz and above to keep input coil noise current </= 0.7pA.

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Notes on original spec, document "990603QETBiasNoiseSpec.PDF" , by J. Hellmig:

A target SQUID noise performance level of 1pA/√Hz was given. A QET resistance of 100mΩ and a Rshunt resistance of 40mΩ was used for a worst case scenario, even though the nominal shunt resistance is 20mΩ. This document will continue to use those values.

The 3U QET bias board Rbias value of 12.5kΩ was used for the spec. The final target noise performance was given as 0.03µV/√Hz at the top of Rbias, which would result in 2.4pA/√Hz bias current noise. For the shunt and sensor resistances given, that would add 0.7pA/√Hz noise current to the input coil, bringing total noise to ~1.2pA/√Hz after adding SQUID noise. The QET bias noise would therefore be allowed to add ~20% to the SQUID noise.

Subsequent to the original spec, the Rbias value was changed from 12.5kΩ 4.99kΩ. This document will continue to use the 2.4pA/√Hz current noise spec and make adjustments for Rbias to keep the voltage spec consistent.

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QET bias spec: <2.4pA/√Hz from 125Hz to 2MHz

This document will use a reverse-engineering analysis of the v1/v2 ZIP board design to determine expected nominal and worst case noise performance of the board. That performance will then be compared to the spec.

ZIP v1 board QET bias analysis and spec:

1) Rbias

The QET Rbias resistor is now 4.99kΩ. In order to meet the 2.4pA/√Hz spec, the noise voltage at the top of Rbias must be:

Vnoise(max) = Rbias*2.4pA = 12nV/√Hz

The Johnson noise of a 4.99kΩ Rbias at 300K is already 9nV/√Hz, so that must be subtracted in quadrature from the total noise to determine the maximum voltage source noise applied to Rbias:

$$Vin(\max) = \sqrt{12nV^2 + 9nV^2} = 7.9\text{nV}/\sqrt{\text{Hz}}$$

2) ZIP v1 QET bias circuit analysis:

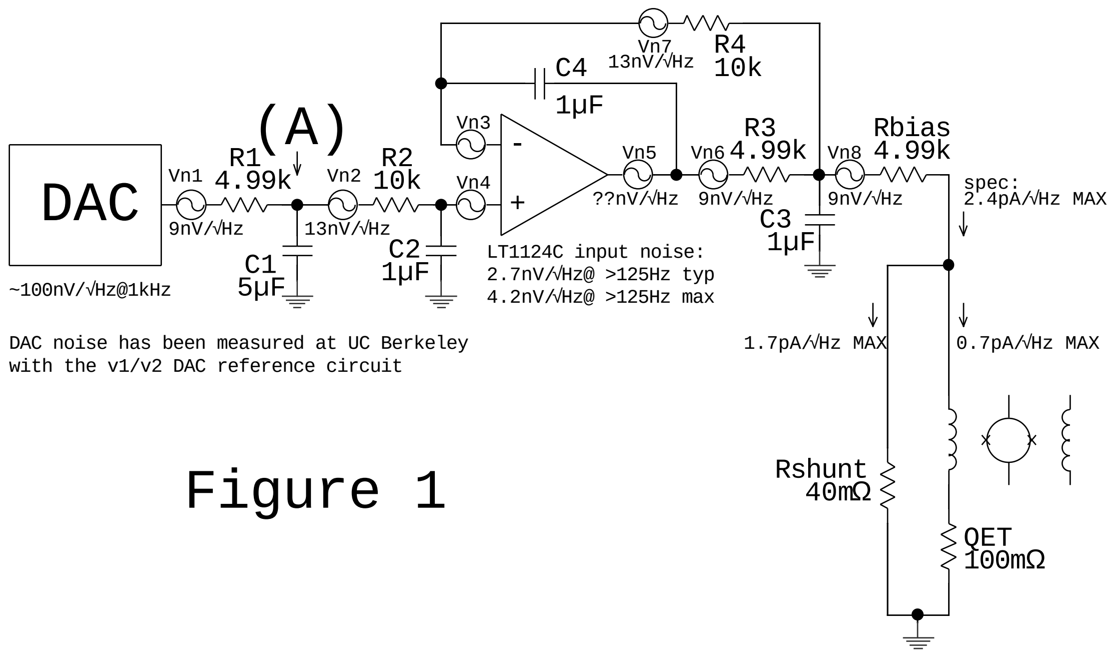
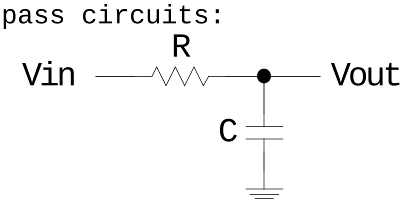


Figure 1

The filters used are RC low pass circuits:



The response of this circuit is –20dB/decade, so at 10X the knee frequency Vout = 0.1Vin, at 100X the knee frequency Vout = 0.01Vin, etc. The output voltage at any particular frequency is given by:

Equation 1:
$$Vout = \frac{Vin}{\sqrt{1 + (2\pi f RC)^2}}$$

First, Vn1 can be ignored because it is so much lower than the DAC noise. In addition, the large value of C1 minimizes interaction between the R1/C1 and R2/C2 networks (Zc1 is 254Ω at 125Hz) so their effects can be considered separately. Using Equation 1, the noise at point A at 125Hz is 5.1nV/√Hz. That noise adds in quadrature with the noise of R2, and is then filtered by R2/C2 to produce only 1.8nV at the output of R2/C2. Noise will be lower still at higher frequencies.

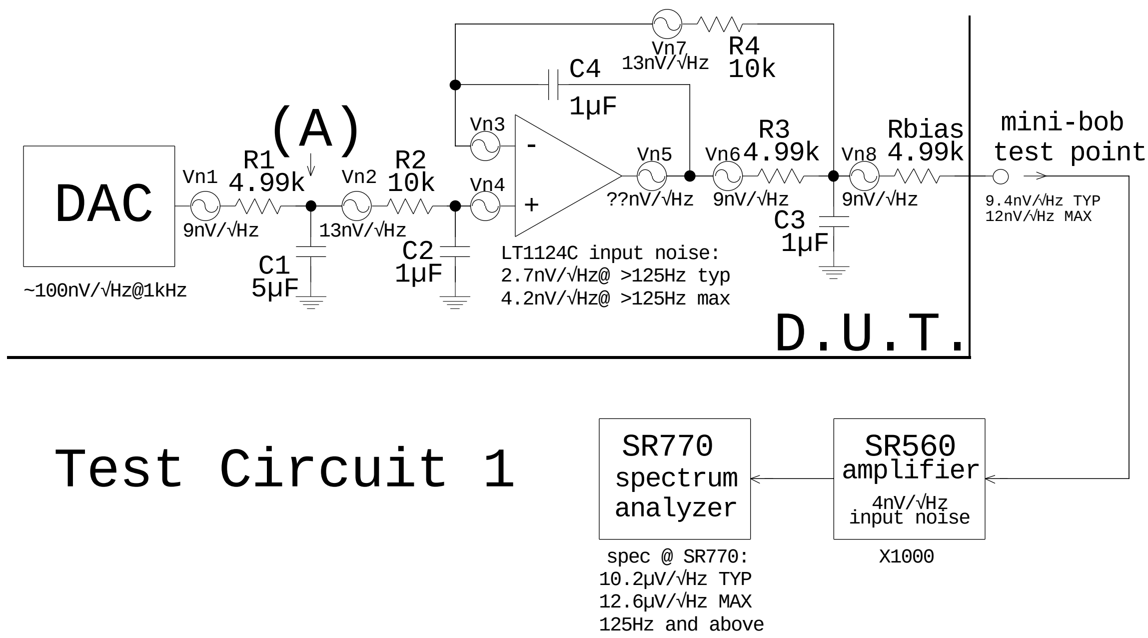
The LT1124C op amp, then, will be the dominant noise source, besides Rbias. The 1.8nV at R2/C2 will add only 10% and can be ignored. The LT1124C input noise should be multiplied by √2 (1.4) since there are two inputs. Total typical input noise, then, is 3.8nV/√Hz and maximum is 5.9nV/√Hz. By themselves these noise sources meet the 7.9nV/√Hz spec, but the output noise of the LT1124C is not specified by the manufacturer and this stage is operated with unity gain.

R4, C4, and R3/C3 act to attenuate the LT1124C noise. C4 provides an AC feedback path directly from the op amp's output, causing the op amp to cancel it's own output noise at frequencies above the R4/C4 time constant (16Hz). R4 provides a DC feedback to set the voltage at the top of Rbias equal to the DAC voltage. Vn7, the noise of R4, is filtered by the R4/C4 time constant. That leaves the op amp input noise and Vn6 as the remaining wide-band noise sources, which are filtered by R3/C3. Equation 1 gives a maximum noise at the top of Rbias of 2.7nV/√Hz at 125Hz. Adding this to Vn8 gives 9.4nV/√Hz and dividing by Rbias gives a final expected current noise of 1.9pA/√Hz.

3)Noise measurement test setup:

Ideally the QET bias noise current would be injected into the input node of the SQUID amp via the mini-bob test board, and changes in the driver output voltage noise measured with the SQUID amp in closed loop operation. This would avoid having to reconfigure test setup connections by always observing the driver output. Unfortunately, the noise contribution of the SQUID amp is much larger than the QET bias contribution and would mask the effect of the QET bias noise, making this approach impractical.

Noise can be measured in units of voltage or current. Voltage noise can be measured directly at the QET bias output pin of the ZIP board or at a mini-bob test point and divided by Rbias to determine the equivalent current noise. This setup is shown in Test Circuit 1, along with nominal and maximum allowable noise specs.



Test Circuit 1